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10/669,040	09/22/2003	Mau-Chung F. Chang	527-28-002	1803

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EXAMINER	
BENGHUZZI, MOHSIN M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,040	CHANG ET AL.	
	Examiner	Art Unit	
	Mohsin (Ben) Benghuzzi M.B.	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17-23 and 28-30* is/are rejected.

7)☒ Claim(s) *15, 16, and 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *22 September 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Line 16, page 25 of the specification contains the characters '???', which are out of context. These characters must be removed and replaced with the appropriate words.

Appropriate correction is required.

Claim Objections

2. Claim 1 is objected to because of the following:

a) In line 15 of the claim, the limitation refers to 'each of said data transmitter circuits,' however, what is claimed in the referenced preceding limitation of line 4 is 'at least one data transmitter circuit.' The term 'at least one' indicates that one data transmitter circuit only may be comprised. The term 'each,' on the other hand, indicates that what is comprised is strictly more than one data transmitter circuits. Examiner suggests that the term 'each' in line 15 of the claim is replaced with 'the at least one.'

b) In line 35 of the claim, the term 'each' should also be replaced accordingly.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, and 18-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Grimwood et al. (US Pub 2001/0033611) and further in view of Yang et al. (US 6,418,537).

1) Regarding claim 1:

Grimwood et al. discloses a source synchronous CDMA bus interface, comprising:

a single data channel ('SHARED MEDIA' in Fig. 1 and paragraph 0048 lines 12-13, wherein, 'SHARED' is interpreted as single channel);

at least one data transmitter circuit coupled to said data channel at a first point (paragraph 0047 lines 5-7 and Fig. 13);

at least one data receiver circuit coupled to said data channel at a second point (paragraph 0047 lines 7-8 and Fig. 24);

each of said data transmitter circuits comprising:

a modulating circuit connected to receive base-band data to be transmitted via said data channel at a first input and a unique orthogonal code at a second input and to produce data modulated by said unique orthogonal code at an output (18 or 54 in Fig. 1 and paragraph 0048 lines 1-7); and

a transmitter connected to receive said modulated data and said first clock at respective inputs and which is arranged to use said first clock to align said modulated data with said system clock signal and to provide said aligned modulated data at an output which is coupled to said data channel at said first point such that said aligned modulated data is transmitted using source synchronous clocking (abstract lines 18-21, paragraph 0048 lines 1-7, and paragraph 0049 lines 5-8, wherein, 'to multiplex' is interpreted as to align);

each of said data receiver circuits comprising:

a receiver coupled to said data channel at said second point such that it receives said aligned modulated data and said second clock at respective inputs and which is arranged to use said second clock to align said received data with said system clock signal (abstract lines 18-21, paragraph 0014 lines 13-14, and paragraph 0016); and

a demodulating circuit connected to receive said aligned received data at a first input and said unique orthogonal code at a second input and to produce data demodulated with said orthogonal code at an output and thereby recover said base-band data (36 or 68 in Fig. 1 and paragraph 0049 lines 1-2).

Grimwood et al. does not disclose:

a system clock line which runs adjacent and parallel to said data channel; and

a system clock signal applied to said system clock line such that said system clock signal propagates in parallel with data sent from said at least one data transmitter circuit to said at least one data receiver circuit via said data channel;

each of said data transmitter circuits comprising:

a first clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to said first point, said first clock generating circuit arranged to generate a first clock signal derived from said system clock signal);

each of said data receiver circuits comprising:

a second clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to said second point, said second clock generating circuit arranged to generate a second clock signal derived from said system clock signal;

However, Yang et al. discloses:

a system clock line which runs adjacent and parallel to said data channel (15_B in Fig. 1A and column 5 lines 53-59); and

a system clock signal applied to said system clock line such that said system clock signal propagates in parallel with data sent from said at least one data transmitter circuit to said at least one data receiver circuit via said data channel (15_B in Fig. 1A and column 5 lines 53-59);

each of said data transmitter circuits comprising:

a first clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to said first point, said first clock generating circuit arranged to generate a first clock signal derived from said system clock signal (2000_A or 2000_B in Fig. 1A);

each of said data receiver circuits comprising:

a second clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to said second point, said second clock generating circuit arranged to generate a second clock signal derived from said system clock signal (100_A or 100_B in Fig. 1A);

It is advantageous that a clock line containing a clock signal runs adjacent and parallel to a data channel. When a clock signal is transmitted on a line separate from the data signal, no clock extraction from the data signal is needed to be done at the receiver, and therefore, eliminating the need for the complex clock extraction circuitry at the receiver. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the interface of Grimwood et al. a system clock and signal that runs adjacent and parallel to the data channel, as Yang et al. teaches, in order to simplify receiver circuitry.

2) Regarding claim 2:

Grimwood et al. discloses the bus interface of claim 1, wherein said first and second clock generating circuits are delay-locked-loop (DLL) circuits (paragraph 0075 and paragraph 0052 lines 4-22).

3) Regarding claim 3:

Grimwood et al. discloses the bus interface of claim 1, wherein said first and second clock generating circuits are phase-locked-loop (PLL) circuits (paragraph 0012 lines 41-54).

4) Regarding claim 18:

Grimwood et al. discloses the bus interface of claim 1, wherein said data channel is a transmission line (paragraph 0012 lines 1-4, wherein, 'cable TV plants' is interpreted as transmission lines).

5) Regarding claim 19:

Grimwood et al. discloses the bus interface of claim 1, further comprising at least one data storage device interfaced to at least one of said data transmitter circuits such that said bus interface provides a memory bus which conveys data from said at least one data storage device to said at least one data receiver circuit (paragraph 0017 lines 25-28).

6) Regarding claim 20:

Grimwood et al. discloses the bus interface of claim 19, further comprising at least one CPU interfaced to at least one of said data receiver circuits such that said memory bus conveys data from said at least one data storage device to said at least one CPU (paragraph 0130 lines 4-9).

7) Regarding claim 21:

Grimwood et al. discloses the bus interface of claim 19, further comprising at least one memory controller interfaced to at least one of said data receiver circuits such that said memory bus conveys data from said at least one data storage device to said at least one memory controller (paragraph 0052 lines 11-13 and paragraph 0200 lines 6-10).

5. Claims 4, 5, 10, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grimwood et al. (US Pub 2001/0033611) and Yang et al. (US 6,418,537), and further in view of Agrawal et al. (US 6,134,215).

1) Regarding claim 4:

Grimwood et al. or Yang et al. do not disclose, wherein said orthogonal codes are Walsh codes. However, Agrawal et al. discloses, wherein said orthogonal codes are Walsh codes (column 13, claim 2).

It is advantageous that Walsh codes are used in a CDMA bus interface. It should be obvious to one skilled in the art that such limitation is desirable. Walsh codes are orthogonal codes that exhibit zero-cross correlation, and thus, easily distinguishable from each other. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Walsh codes as the orthogonal codes in the interface of Grimwood et al. and Yang et al., in order to have codes that are easily distinguishable.

2) Regarding claim 5:

Grimwood et al. or Yang et al. do not disclose, wherein said at least one data transmitter circuit and said at least one data receiver circuit comprise at least two data transmitter circuits and at least two data receiver circuits, each of said modulating circuits receiving respective unique orthogonal codes and each of said demodulating circuits corresponding to one of said modulating circuits and receiving said modulating circuit's orthogonal code, said unique orthogonal codes enabling the aligned modulated data from said at least two data transmitter circuits to be conveyed via said single data

channel to said at least two data receiving circuits simultaneously. However, Agrawal et al. discloses, wherein said at least one data transmitter circuit and said at least one data receiver circuit comprise at least two data transmitter circuits and at least two data receiver circuits, each of said modulating circuits receiving respective unique orthogonal codes and each of said demodulating circuits corresponding to one of said modulating circuits and receiving said modulating circuit's orthogonal code, said unique orthogonal codes enabling the aligned modulated data from said at least two data transmitter circuits to be conveyed via said single data channel to said at least two data receiving circuits simultaneously (column 10 lines 46-51, wherein, 'multiple transmitters and multiple receivers' is interpreted as at least two data transmitter circuits and at least two data receiver circuits. See also column 12 lines 51-53, column 7 lines 12-16, and column 14 lines 60-61).

3) Regarding claim 10:

Grimwood et al. discloses, further comprising a system controller which provides said unique orthogonal codes to said data transmitter circuits and said data receiving circuits such that aligned modulated data coupled to said data channel is received and demodulated by a specific data receiver circuit, said system controller thereby configuring said bus interface (paragraph 0084 lines 4-6, paragraph 0014 lines 13-14, and paragraph 0267).

4) Regarding claim 17:

Agrawal et al. further discloses, wherein said data channel is parallel terminated at each end (column 14 claim 23, wherein, in lines 60-61 'receiving at least two user signals sharing a single channel' is interpreted as parallel termination of data channel).

6. Claims 6-9, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grimwood et al. (US Pub 2001/0033611), Yang et al. (US 6,418,537), and Agrawal et al. (US 6,134,215), and further in view of Schilling (US 5,274,665).

1) Regarding claim 6:

Grimwood et al. or Yang et al. or Agrawal et al. do not disclose, wherein said at least two data transmitter circuits share said first clock signal and the outputs of said at least two data transmitter circuits are connected together at a common node which is coupled to said data channel at said first point. However, Schilling discloses, wherein said at least two data transmitter circuits share said first clock signal and the outputs of said at least two data transmitter circuits are connected together at a common node which is coupled to said data channel at said first point (column 14 lines 46-52 and lines 54-58).

It is desirable that a multiple transmitter circuits share a clock signal. Use of only one clock signal does not require that multiple clock signals be synchronized and is also cost and space efficient. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the data transmitter circuits of Grimwood et al., Yang et al., and Agrawal et al. share a first clock signal, as Schilling

discloses, in order to result in a bus interface that does not require multiple clock signals synchronization and is cost and space efficient.

2) Regarding claim 7:

Schilling discloses, wherein the outputs of said at least two data transmitter circuits are coupled to said data channel at different points along said data channel, each of said data transmitter circuits having respective first clock circuits, the input of each first clock circuit connected to said system clock line at a point approximately adjacent to where said first clock circuit's data transmitter circuit is coupled to said data channel, such that the outputs of said data transmitter circuits are transmitted using source synchronous clocking and superposed in said data channel (column 10 lines 42-44, column 20 lines 40-60, and column 14 lines 46-52, lines 54-58).

3) Regarding claim 8:

Schilling discloses, wherein said at least two data receiver circuits share said second clock signal and the inputs of said at least two data receiver circuits are connected together at a common node which is coupled to said data channel at said second point (column 14 lines 46-52, lines 54-58 and column 11 lines 3-25).

4) Regarding claim 9:

Schilling discloses, wherein the inputs of said at least two data receiver circuits are coupled to said data channel at different points along said data channel, each of said data receiver circuits having respective second clock circuits, the input of each second clock circuit connected to said system clock line at a point approximately adjacent to where said second clock circuit's data receiver circuit is coupled to said data

channel (column 11 lines 3-25, column 11 line 47 to column 12 line 17, and column 14 lines 46-52, lines 54-58).

5) Regarding claim 22:

Schilling further discloses, wherein said modulating circuit comprises at least one exclusive-OR gate connected to receive said base-band data and said unique orthogonal code at respective inputs and to produce said modulated data at said output (column 10 lines 31-32), said modulated data cd0(t) given by:

$cd0(t) = D0(t) + C0(t)$,

7. Claims 11-14 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grimwood et al. (US Pub 2001/0033611), Yang et al. (US 6,418,537), and Agrawal et al. (US 6,134,215), and further in view of Doyle (US 5,856,980).

1) Regarding claim 11:

Grimwood et al. or Yang et al. or Agrawal et al. do not disclose, wherein said at least two data transmitter circuits and said at least two data receiver circuits comprise two data transmitter circuits and two data receiver circuits which are arranged such that said aligned modulated data employs 3-PAM signaling when data from said two data transmitter circuits is simultaneously conveyed via said single data channel to said two data receiver circuits. However, Doyle discloses, wherein said at least two data transmitter circuits and said at least two data receiver circuits comprise two data transmitter circuits and two data receiver circuits which are arranged such that said

aligned modulated data employs 3-PAM signaling when data from said two data transmitter circuits is simultaneously conveyed via said single data channel to said two data receiver circuits (column 14 lines 4-11, wherein, 'three or more levels' is interpreted as three levels, i.e., 3-PAM signaling).

It is advantageous to employ 3-PAM signaling and not higher level signaling. 3-PAM signaling produces lower data rate, and thus, less channel bandwidth is needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ 3-PAM signaling, as Doyle teaches, in the interface of Grimwood et al., Yang et al., and Agrawal et al., in order to result in less channel bandwidth requirement.

2) Regarding claim 12:

As discussed in claim 4 above, Agrawal et al. discloses, wherein said orthogonal codes are 2-bit Walsh codes (column 5 lines 40-43, wherein, 'n' is interpreted to be 2).

3) Regarding claim 13:

As discussed in claim 5 above, Agrawal et al., discloses, wherein said at least two data transmitter circuits and said at least two data receiver circuits comprise four data transmitter circuits and four data receiver circuits (column 10 lines 46-51, wherein, 'multiple transmitters and multiple receivers' is interpreted as four data transmitter circuits and four data receiver circuits. See also column 12 lines 51-53, column 7 lines 12-16, and column 14 lines 60-61).

Regarding, which are arranged such that said aligned modulated data employs 5-PAM signaling when data from said four data transmitter circuits is simultaneously

conveyed via said single data channel to said four data receiver circuits, as discussed in claim 11 above, Doyle discloses, which are arranged such that said aligned modulated data employs 5-PAM signaling when data from said four data transmitter circuits is simultaneously conveyed via said single data channel to said four data receiver circuits (column 14 lines 4-11, wherein, 'three or more levels' is interpreted as five levels, i.e., 5-PAM signaling).

4) Regarding claim 14:

As discussed in claim 4 above, Agrawal et al. discloses, wherein said orthogonal codes are 4-bit Walsh codes (column 5 lines 40-43, wherein, 'n' is interpreted to be 4).

5) Regarding claim 28:

Grimwood et al. discloses a source synchronous CDMA bus interface suitable for use as a memory bus which provides 2-to-2 multiple access communications, comprising:

a single data channel ('SHARED MEDIA' in Fig. 1 and paragraph 0048 lines 12-13, wherein, 'SHARED' is interpreted as single channel);

each of said data transmitter circuits comprising:

a modulating circuit connected to receive base-band data to be transmitted at a first input and a unique orthogonal code at a second input and to produce data modulated by said unique orthogonal code at an output (18 or 54 in Fig. 1 and paragraph 0048 lines 1-7); and

a transmitter connected to receive said modulated data and said first clock at respective inputs and which is arranged to use said first clock to align said modulated

data with said system clock signal and to provide said aligned modulated data at an output which is coupled to said data channel such that said aligned modulated data is transmitted using source synchronous clocking (abstract lines 18-21, paragraph 0048 lines 1-7, and paragraph 0049 lines 5-8, wherein, 'to multiplex' is interpreted as to align);

each of said data receiver circuits comprising:

a receiver coupled to said data channel such that it receives said aligned modulated data and said second clock at respective inputs and which is arranged to use said second clock to align said received data with said system clock signal (abstract lines 18-21, paragraph 0014 lines 13-14, and paragraph 0016); and

a demodulating circuit connected to receive said aligned received data at a first input and the orthogonal code provided to a given one of said modulating circuits at a second input and to produce data demodulated with said orthogonal code at an output, thereby recovering the base-band data modulated by said given modulating circuit (36 or 68 in Fig. 1 and paragraph 0049 lines 1-2).

As discussed in claim 5 above, Agrawal et al. discloses, first and second data transmitter circuits coupled to said data channel (column 10 lines 46-51, wherein, 'multiple transmitters' is interpreted as first and second data transmitter circuits. See also column 12 lines 51-53, column 7 lines 12-16, and column 14 lines 60-61).

As discussed in claim 5 above, Agrawal et al. discloses, first and second data receiver circuits coupled to said data channel (column 10 lines 46-51, wherein, 'multiple

receivers' is interpreted as first and second data receiver circuits. See also column 12 lines 51-53, column 7 lines 12-16, and column 14 lines 60-61).

As discussed in claim 1 above, Yang et al. discloses:

a system clock line which runs adjacent and parallel to said data channel (15_B in Fig. 1A and column 5 lines 53-59); and

a system clock signal applied to said system clock line such that said system clock signal propagates in parallel with data sent from said data transmitter circuits to said data receiver circuits via said data channel (15_B in Fig. 1A and column 5 lines 53-59);

each of said data transmitter circuits comprising:

a first clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to where said data transmitter circuit is coupled to said data channel, said first clock generating circuit arranged to generate a first clock signal derived from said system clock signal (2000_A or 2000_B in Fig. 1A);

each of said data receiver circuits comprising:

a second clock signal generating circuit coupled at its input to said system clock line at a point approximately adjacent to where said data receiver circuit is coupled to said data channel, said second clock generating circuit arranged to generate a second clock signal derived from said system clock signal (100_A or 100_B in Fig. 1A).

As discussed in claim 11 above, Doyle discloses, said data transmitter circuits coupling their respective aligned modulated data into said data channel simultaneously

such that said data is transmitted using 3-PAM signaling (column 14 lines 4-11, wherein, 'three or more levels' is interpreted as three levels, i.e., 3-PAM signaling).

6) Regarding claim 29:

Grimwood et al. discloses, wherein said first and second clock generating circuits are delay-locked-loop (DLL) circuits (paragraph 0075 and paragraph 0052 lines 4-22).

7) Regarding claim 30:

As discussed in claim 4 above, Agrawal et al. discloses, wherein said orthogonal codes are 2-bit Walsh codes (column 5 lines 40-43, wherein, 'n' is interpreted to be 2).

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grimwood et al. (US Pub 2001/0033611) and Yang et al. (US 6,418,537), and further in view of Fiedler et al. (US 6,490,325).

Grimwood et al. or Yang et al. do not disclose, wherein said transmitter comprises an output driver having a current-mode open-drain structure. However, Fiedler et al. discloses, wherein said transmitter comprises an output driver having a current-mode open-drain structure (column 1 lines 24-27 and column 4 lines 60-65).

It is desirable that the output driver of a transmitter has a current-mode open-drain structure. Current-mode open-drain drivers have a high output resistance, and thus, have less effect on a transmission line to which a transmitter is coupled (see Fiedler et al., column 1 lines 24-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the transmitter of Grimwood et al. and Yang et al. comprise an output driver that has a current-mode

open-drain structure, as Fiedler et al teaches, in order for the transmitter to have less effect on the transmission line.

Allowable Subject Matter

10. Claims 15, 16, and 24-27 are objected to as being dependent upon a rejected base claim. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record also fails to clearly teach or suggest a system clock line that runs adjacent and parallel to a data channel in a first direction, reverses direction and continues adjacent and parallel to the data channel in a second direction opposite to the first direction. The prior art of record also fails to clearly teach or suggest that the aligned modulated data from the two data transmitter circuits is transmitted through a single data channel to two data receiving circuits simultaneously using 3-PAM signaling, wherein, the receiving circuits comprise first and second 2-bit ADCs for handling even and odd data, respectively, wherein, each of said 2-bit ADCs receiving two DC reference voltages such that the ADC converts said 3-PAM signal to thermometer coded data and to integrate said coded data.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Feher (US 7,035,344) discloses a transceiver system for modulation-demodulation for high spectral efficient signal generation.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached Monday through Friday, 8:30am- 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M. G.

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER

Mohsin (Ben) Benghuzzi February 15, 2007